REMARKS

In accordance with the foregoing, claims 18-34 have been cancelled without prejudice or disclaimer.

Claims 1-17 are pending and under consideration.

OBJECTION TO THE CLAIMS

On page 2 of the Office Action, claims 18-22 are objected to as being substantial duplicate of claims 1-17. Claims 18-22 are cancelled herewith without prejudice or disclaimer. Accordingly, it is respectfully requested that the objections to the claims be withdrawn.

REJECTION UNDER 35 U.S.C. § 103:

On page 2 of the Office Action, claims 1 and 5 are rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,067,611 to Carpenter ("Carpenter") and U.S. Patent No. 6,263,405 to Irie ("Irie").

As noted in the Office Action, Carpenter does not show the use of a preread (or speculative read) and a buffer within the crossbar module to hold the data preread from a system module other than the arbitrary system module. The Office Action accordingly relies on Irie as showing the use of a preread and a buffer within the crossbar module to hold the data preread from a system module other than the arbitrary system module.

On page 15, line 9, of the Office Action, the following is stated: "preread has been interpreted by the examiner as issuing simultaneous requests to different memories for the same data." Applicants respectfully assert that the term "preread," as appears in the phrase "holding data preread from a system module" is incorrectly interpreted by the Examiner to define "preread", as appears in the phrase "issuing simultaneous requests to different memories..." For instance, according to an aspect of the present invention, a multiprocessor holds preread data at a location which is as close as possible to a processor which made a read request, so that it is possible to bring out the advantageous effects of the data preread access without interfering with the normal data transfer, thereby improving the performance of the multiprocessor system as a whole. Thus, the claims of the presently claimed invention have been incorrectly interpreted in view of the cited references.

As correctly noted by the Examiner, Carpenter fails to teach or suggest "holding data preread from a system module, other than the arbitrary system module, in a buffer within the

crossbar module," as recited in independent claim 1. Thus, Irie is relied upon as teaching such claimed features.

However, it must be noted that Irie merely proposes (1) a queuing buffer (FIFO) within a crossbar unit, and (2) prereading from a memory and queuing within a memory board or (3) prereading from a memory and transferring the preread data to a processor board for queuing within the processor board (by the buffer).

In contrast, according to an aspect of the present invention, (a) a buffer is used (data buffer which can change the transfer sequence) within a crossbar module, and (b) prereads and transfers the preread data from a system module to the crossbar module (by lowering the priority if necessary) for queuing within the crossbar module. Features (a) and (b) of the present invention are completely different from the features (1), and (2) or (3) of Irie as described above.

Regarding the prereading, Irie describes the buffering within the memory board and the possibility of transferring the preread data to the processor board (See column 18, lines 25-49 of Irie). Although Irie appears to describe a crossbar unit, Irie does not teach or even suggest "responsive to a read request from a processor within an arbitrary system module, holding data preread from a system module, other than the arbitrary system module, in a buffer within the crossbar module," as recited in independent claim 1.

In addition, FIGS. 9 and 10 are referred to in the Office Action. However, it must be noted that in Irie, it is always the memory board that receives the transfer enable/disable (permit/prohibit), and **not** the crossbar unit.

On the other hand, in the present invention, the transfer enable/prohibit is received by a destination point of the preread data transfer, including the crossbar module. It is not obvious, even to those skilled in the art, to carry out the queuing/priority assignment of the memory preread within the crossbar module.

Furthermore, as may bee seen on FIG. 6 of Iris, which illustrates the crossbar unit, the data queue (INQ) has a FIFO (in-order) structure for each port, and it is clear that Irie cannot lower the priority by reversing the order for the memory preread. However, according to an aspect of the present invention, the priority may be lowered in the crossbar module (See claim 3, reciting "adding, to a data transfer of the preread data, a priority which is lower than a priority of a normal data transfer," for instance) because the priority order control maintains the cache coherency.

Thus, according to an aspect of the present invention, it is possible to freely carry out the queuing within the processor, the system module, and the crossbar module, which is very different from Irie, which can carry out the queuing only within the memory board. Even if we assumed, *arguendo*, that Irie suggests carrying out the queuing within the processor board, Irie still does not teach or suggest a structure that enables the queuing location to be selected dynamically as done in the present invention. The present invention enables efficient data transfer because the queuing location can be selected dynamically by assigning an arbitrary priority order.

Furthermore, in Irie, in a crossbar unit 40 multicasts a data read transaction to all the processor boards 10-0 to 10-1 and to a specified memory board 60-0 (step 904). See column 6, line 44, to column 7, line 12 of Irie. A coherency status report sum-up unit 50 makes a summary of the coherency status reports when it receives all the coherency status reports, and sends the coherency status summary CSS to the coherent read requesting processor board 10-0.

At the same time, the sum-up unit sends a memory data transfer allowance signal to the memory board 60-0, which receives the coherent read request and **accesses the internal main memory 61**. (Emphasis added) Thus, rather than "holding data preread from a system module, other than the arbitrary system module, in a buffer within the crossbar module," as recited in independent claim 1, when the memory board 60-0 receives the transfer allowance signal from the coherency status report sum-up unit 50, the memory board sends **the retrieved data as a data transaction** to the crossbar unit 40 (step 908). (Emphasis added)

Accordingly, rather than holding data preread from the system module, the crossbar unit 40 transfers the data transaction to the processor board 10-0 which issued the coherent read request (step 909).

FIG. 6 of Irie is a block diagram of a crossbar unit. However, neither in FIG. 6 nor in the corresponding description is there a teaching or suggestion of a buffer. In particular, FIG. 6 of Irie falls to teach or suggest, "holding data preread from a system module . . . in a buffer within the crossbar module," as recited in independent claim 1.

The Office Action refers to column 7, lines 3-6, as describing the buffer in the crossbar unit 40. However, the referenced portion of Irie merely describes receiving the transfer allowance signal from the coherency status report sum-up unit 50 and the memory board sending the retrieved data (i.e., data normally read in the multiprocessor system) as a data transaction to the crossbar unit 40 or sending the latest data read out (i.e., the data normally

read) from the cache 12 as a data transaction to the crossbar unit 40.

Applicants respectfully submit that making a summary of the coherency status reports for the normal read, as in Irie, column 6, line 44, to column 7, line 12, is completely different from holding the data preread from a system module other than the arbitrary system module in accordance with the present invention.

Independent claim 5 recites, "said crossbar module including a buffer which holds data preread from a system module, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module." Because independent claim 5 includes similar recitations as those recited in independent claim 1, although of different scope, the arguments presented above supporting the patentability of independent claim 1 are incorporated herein to support the patentability of independent claim 5.

On page 5 of the Office Action, claims 2 and 6 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,055,650 to Christie ("Christie").

Because claims 2 and 6 depend from independent claims 1 and 5, respectively, Carpenter, Irie, and Christie, individually or combined, must teach all the claimed features of independent claims 1 and 5. The arguments presented above supporting the patentability of independent claims 1 and 5 in view of Carpenter and Irie are incorporated herein.

Christie generally describes detecting a phase change in a program being executed and reducing a number of prefetching operations. A prefetch unit is configured to selectively prefetch in response to the detected phase changes. See column 2, lines 36-67, and column 5, line 51, to column 6, line 35 of Christie. However, similarly to Carpenter and Irie, Christie fails to teach or suggest, "responsive to a read request from a processor within an arbitrary system module, holding data preread from a system module, other than the arbitrary system module, in a buffer within the crossbar module," as recited in independent claim 1. Christie is silent as to providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module. Thus; Carpenter, Irie, and Christie, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 1.

Because independent claim 5 includes similar recitations as those of independent claim 1, although of different scope, the arguments presented above supporting the patentability of

independent claim 1 are incorporated herein to support the patentability of independent claim 5.

On page 6 of the Office Action, claims 4, 8, and 12-15 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 5,761,452 to Hooks ("Hooks").

Because claims 4, 8, and 12-15 depend from independent claims 1 and 5, Carpenter, Irie, and Hooks, individually or combined, must teach all the claimed features of independent claims 1 and 5. The arguments presented above supporting the patentability of independent claims 1 and 5 in view of Carpenter and Irie are incorporated herein.

Hooks generally describes a bus arbiter method assigning a priority to a requesting master when a pre-fetch signal is or is not asserted. See column 5, lines 18-25 of Hooks. However, the cited reference, similarly to Carpenter and Irie, fails to teach or suggest, "responsive to a read request from a processor within an arbitrary system module, holding data preread from a system module, other than the arbitrary system module, in a buffer within the crossbar module," as recited in independent claim 1. Hooks is silent as to providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module. Thus, Carpenter, Irie, and Hooks, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 1.

The Office Action provides absolutely no motivation to combine the cited references. Rather, conclusive statements are made, such as "it is obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks." However, "rejection of patent application for obviousness under 35 USC §103 must be based on evidence comprehended by language of that section, and search for and analysis of prior art includes evidence relevant to finding of whether there is teaching, motivation, or suggestion to select and combine references relied on as evidence of obviousness; factual inquiry whether to combine references must be thorough and searching, based on objective evidence of record." See In re Lee 61 USPQ2d 1430 (CA FC 2002).

Thus, as pointed out in In re Lee, the record must support motivation, i.e., there must be something in the record pointing out where the recited motivation can be found. In addition, there must be some discussion on how that purported motivation or suggestion is even relevant to the reference being modified. However, nothing in either Carpenter or Irie provides a need for including in their respective systems a determination of a transaction that needs to be performed versus a transaction that might be performed as in Hooks.

Only the present invention sets forth all the claimed features, as well as the motivation for combining the same. The outstanding rejection would appear to have taken this teaching of the present invention and applied the same to produce the combination of Carpenter, Irie, and Hooks, as set forth in the Office Action, to disclose the presently claimed invention. Applicants respectfully indicate that the prima facie burden has not been met and the obviousness rejection fails on its face.

Because independent claim 5 includes similar recitations as those recited in independent claim 1, although of different scope, the arguments presented above supporting the patentability of independent claim 1 are incorporated herein to support the patentability of independent claim 5.

On page 7 of the Office Action, claims 3 and 7are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, Christie, and Hooks.

Because claims 3 and 7 depend from independent claims 1 and 5, respectively, Carpenter, Irie, Christie, and Hooks, individually or combined, must teach all the claimed features of independent claims 1 and 5. The arguments presented above supporting the patentability of independent claims 1 and 5 in view of Carpenter, Irie, Christie, and Hooks are incorporated herein.

Further, Applicants incorporate herein the arguments presented above for improper motivation in combining the references.

On page 9 of the Office Action, claim 9 was rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,341,337 to Pong ("Pong").

Because claim 9 depends from independent claim 5, respectively, Carpenter and Irie, individually or combined, must teach all the claimed features of independent claim 5. The arguments presented above supporting the patentability of independent claim 5 in view of Carpenter and Irie are incorporated herein.

Pong generally describes determining whether a node should transmit a requested data block to an initiator node in response to a read miss transaction transmitted through a snoop bus. The requested data block is only fetched from main memory and returned to the initiator node when no other node has a modified copy of the data block. In this manner, the bus traffic is reduced since only the valid copy of the requested data item is transmitted to the initiator node. See column 7, lines 25-67 of Pong. However, similarly to Carpenter and Irie, Pong fails to

teach or suggest, "said crossbar module including a buffer which holds data preread from a system module, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module," as recited in independent claim 5. Pong is silent as to providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module. Thus, Carpenter, Irie, and Pong, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 5.

The Office Action furthermore fails to establish *prima facie* obviousness of the combination relied upon.

On page 10 of the Office Action, claims 10-11 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,263,415 to Venkitakrishnan ("Venkitakrishnan").

Because claim 10 depends from independent claim 5, Carpenter, Irie, and Venkitakrishnan, individually or combined, must teach all the claimed features of independent claim 5. The arguments presented above supporting the patentability of independent claim 5 in view of Carpenter and Irie are incorporated herein.

Venkitakrishnan generally describes a backup redundant routing system providing a crossbar switch using a plurality of chips. Nodes 200, 300, 400, and 500 are connected to crossbar switches 600 and 700, providing a flexible structure that allows dynamic programming of the data routing and enable support of different network architectures. See column 3, lines 7-38 of Venkitakrishnan. However, similarly to Carpenter and Irie, Venkitakrishnan fails to teach or suggest, "said crossbar module including a buffer which holds data preread from a system module, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module," as recited in independent claim 5. Venkitakrishnan fails to teach or suggest providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module. Thus, Carpenter, Irie, and Venkitakrishnan, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 5.

Referring to independent claim 11, Carpenter, Irie, and Venkitakrishnan, individually or combined, fail to teach or suggest, "each of the system modules including a buffer which holds data, a plurality of processors each having a cache memory which temporarily holds data, and a control unit which controls input and output of data with respect to the system

module to which the control unit belongs," as recited in independent claim 11. The combination of the references fails to appreciate all the claimed features recited in the presently claimed invention. For instance, the combination of the references fails to teach or suggest providing a crossbar module, a buffer in the crossbar module; and holding data preread from a system module in the buffer of the crossbar module.

The Office Action furthermore fails to establish prima facie obviousness of the combination relied upon. As pointed out in In re Lee, the record must support motivation, i.e., there must be something in the record pointing out where the recited motivation can be found. In addition, there must be some discussion on how that purported motivation or suggestion is even relevant to the reference being modified. However, nothing in either Carpenter or Irie provide a need for a reduction of signal lines between crossbars and for easy of expandability as in Venkitakrishnan.

Only the present invention sets forth all the claimed features, as well as the motivation for combining the same. The outstanding rejection would appear to have taken this teaching of the present invention and applied the same to generate a combination of Carpenter, Irie, and Venkitakrishnan, as set forth in the Office Action, allegedly rendering obvious the presently claimed invention. Applicants respectfully assert that prima facie obviousness has not been shown and, thus, the obviousness rejection fails on its face.

On page 12 of the Office Action, claims 16 and 17 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, Venkitakrishnan, and Hooks.

Because claims 16 and 17 depend from independent claim 11, Carpenter, Irie, Venkitakrishnan, and Hooks, individually or combined, must teach all the claimed features of independent claim 11. The arguments presented above supporting the patentability of independent claim 11 in view of Carpenter, Irie, and Venkitakrishnan are incorporated herein.

Hooks, similarly to Venkitakrishnan, Carpenter, and Irie, fails to teach or suggest, "each of the system modules including a buffer which holds data, a plurality of processors each having a cache memory which temporarily holds data, and a control unit which controls input and output of data with respect to the system module to which the control unit belongs," as recited in independent claim 11. In particular, Hooks is silent as to providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module. Thus, Carpenter, Irie, Venkitakrishnan, and Hooks, individually or combined, fail to teach or suggest all the claimed features recited in independent

claim 11.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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